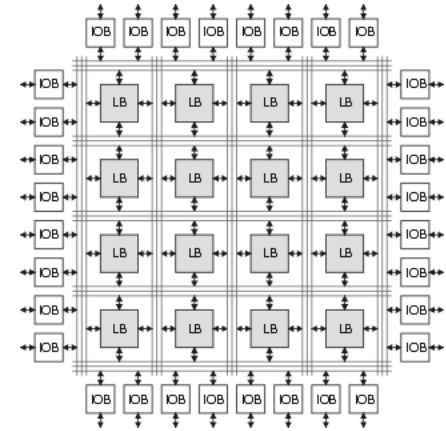
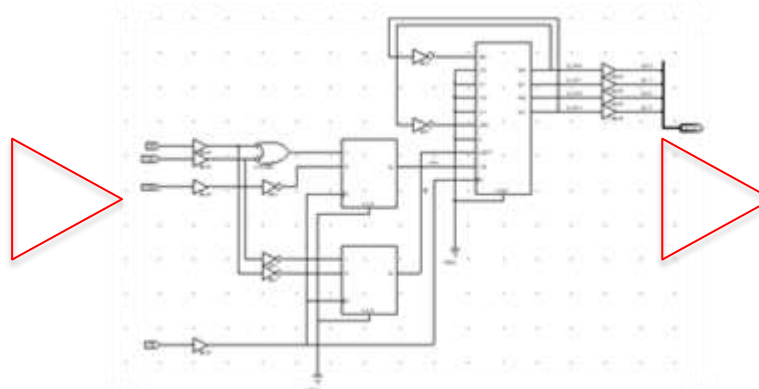


```

begin
  if (RESET_N = '0') then
    for col in 0 to BOARD_COLUMNS-1 loop
      for row in 0 to BOARD_ROWS-1 loop
        ...
      elsif (rising_edge(CLOCK)) then
        ...
      end loop
    end loop
  end if
end

```



Laboratorio di Sistemi Digitali M

A.A. 2010/11

2 – Introduzione Altera Quartus II e schede di sviluppo Altera-Terasic DE1

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Altera Quartus II

- Quartus II è l'ambiente di sviluppo della Altera, che consente la progettazione di sistemi digitali sia in modalità grafica (block diagram) che testuale (VHDL ed altri)

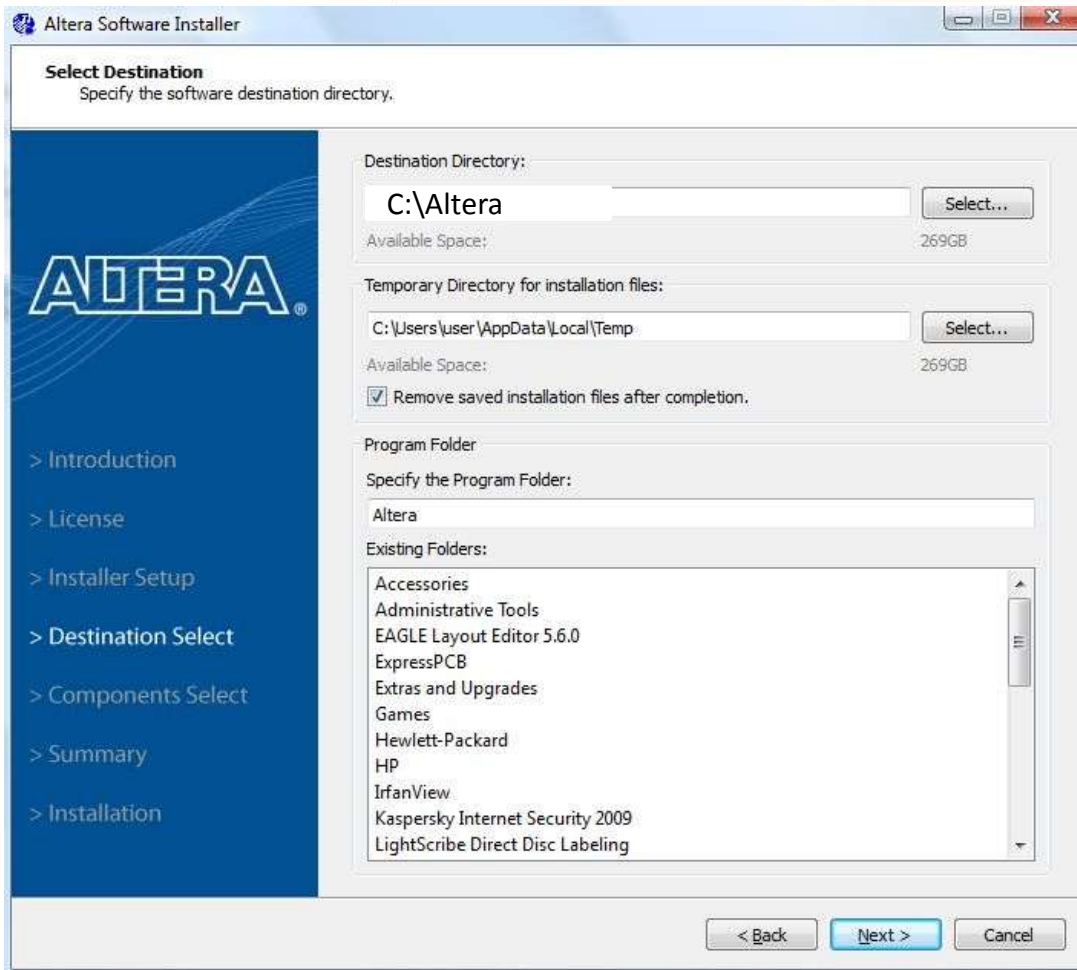
Versione gratuita: Altera Quartus II *Web Edition*

<http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html>



Per le esercitazioni servirà solo Quartus II (potete evitare di installare ModelSim e NIOS)

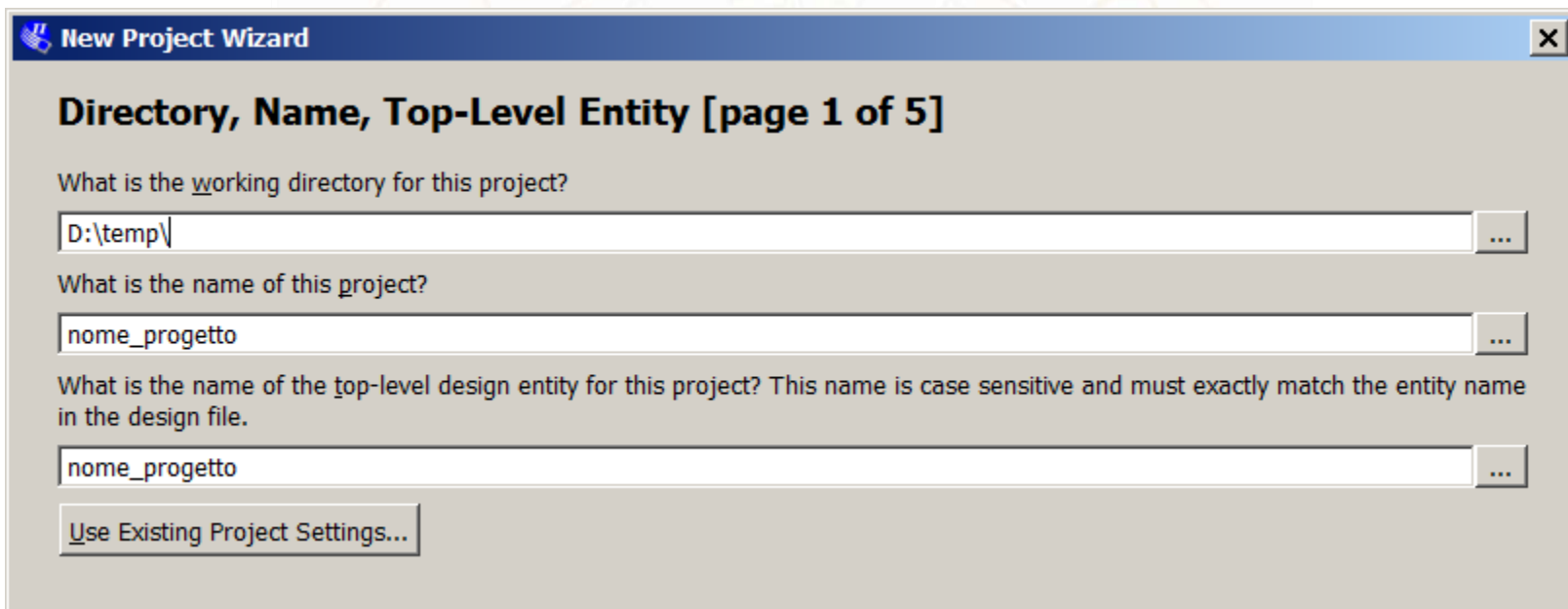
Installazione Quartus II



- Installate in C:\Altera\
(evitate \Program Files o directory con spazi. Molti script della Altera hanno problemi a riguardo)
- Nelle opzioni del setup potete selezionare solo la famiglia Cyclone II per risparmiare spazio sul disco.

Quartus II – Getting started

- New project wizard (1/5)



New Project Wizard [X]

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

D:\temp\ ...

What is the name of this project?

nome_progetto ...

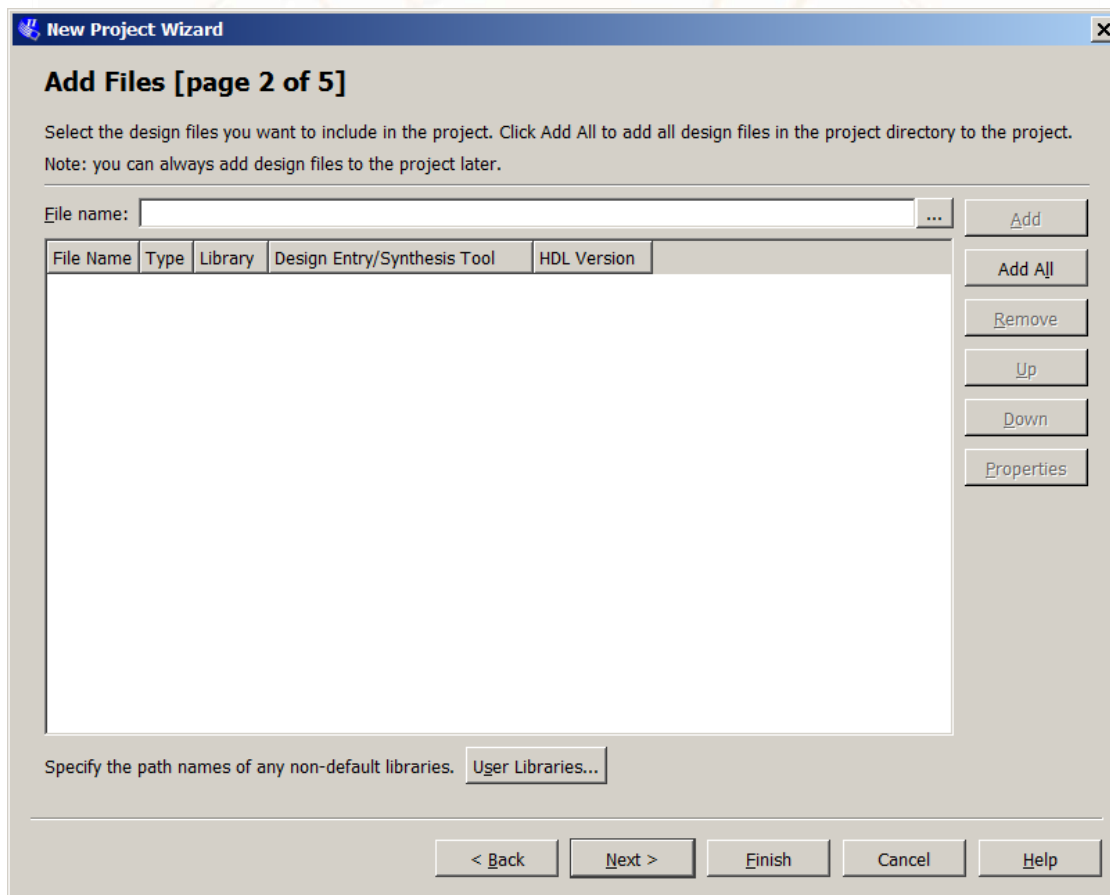
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

nome_progetto ...

Use Existing Project Settings...

Quartus II – Getting started

- Add files (2/5) : lasciate in bianco



Quartus II – Getting started

- Family & Device settings (3/5). Family: Cyclone II. **EP2C20F484C7**

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone II

Devices: All

Target device

Auto device selected by the Fitter

Specific device selected in 'Available devices' list

Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Show advanced devices

HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements
EP2C20F484C6	1.2V	18752	315	239616	52
EP2C20F484C7	1.2V	18752	315	239616	52
EP2C20F484C8	1.2V	18752	315	239616	52

Companion device

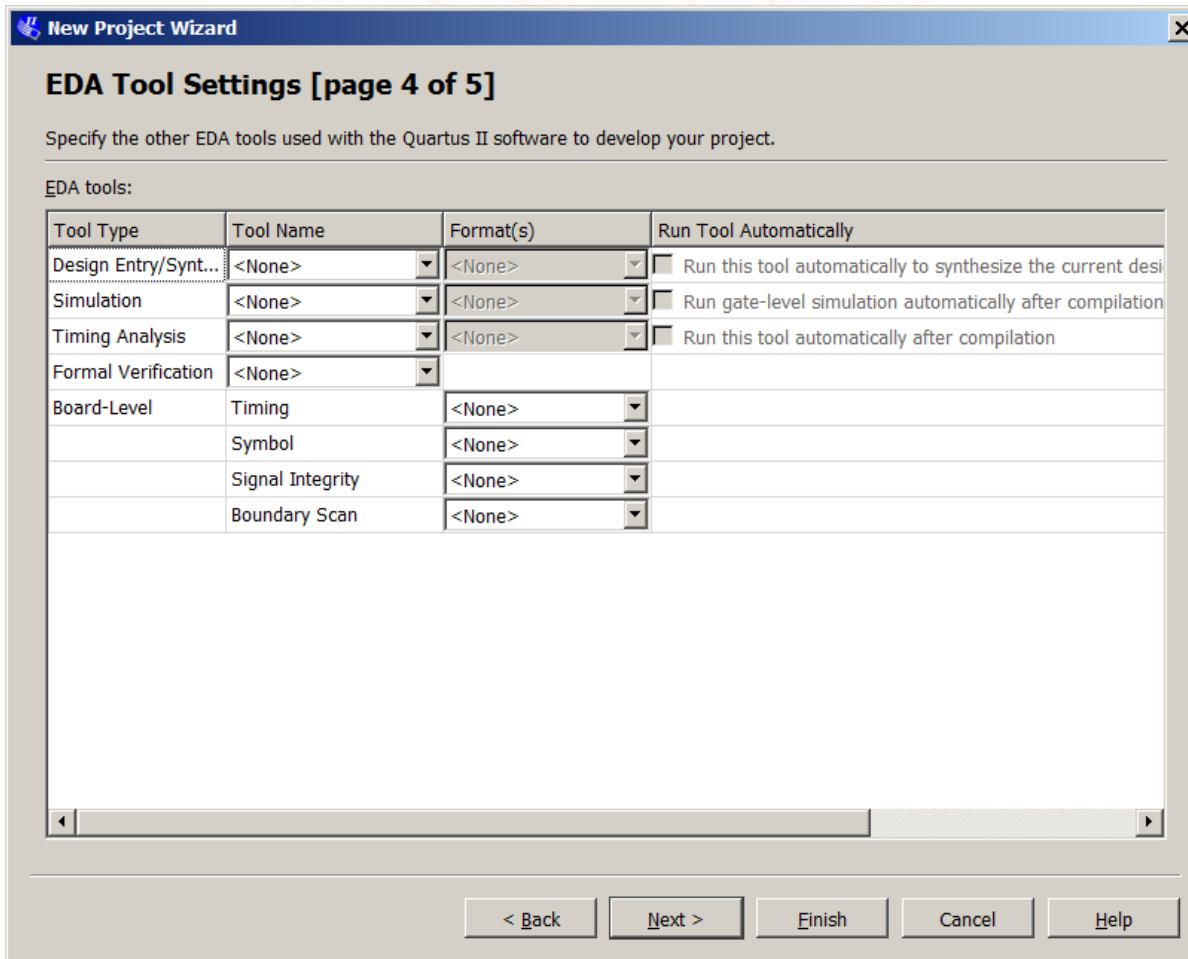
HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Quartus II – Getting started

- EDA Tool Settings (4/5). Lasciate in bianco → Finish



New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

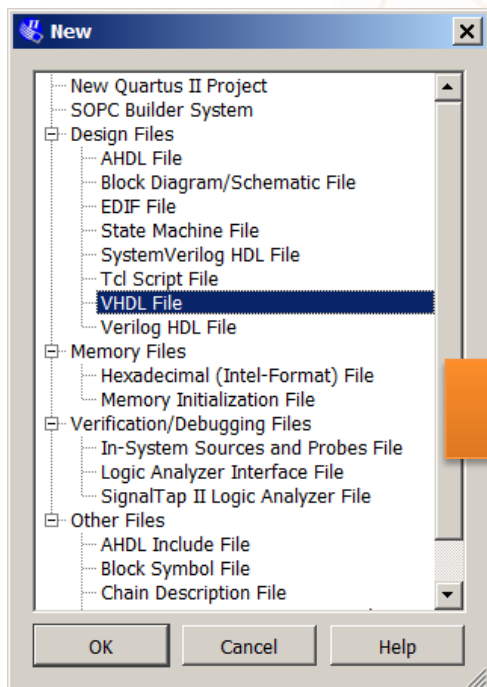
EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synt...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current desi
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Timing Analysis	<None>	<None>	<input type="checkbox"/> Run this tool automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

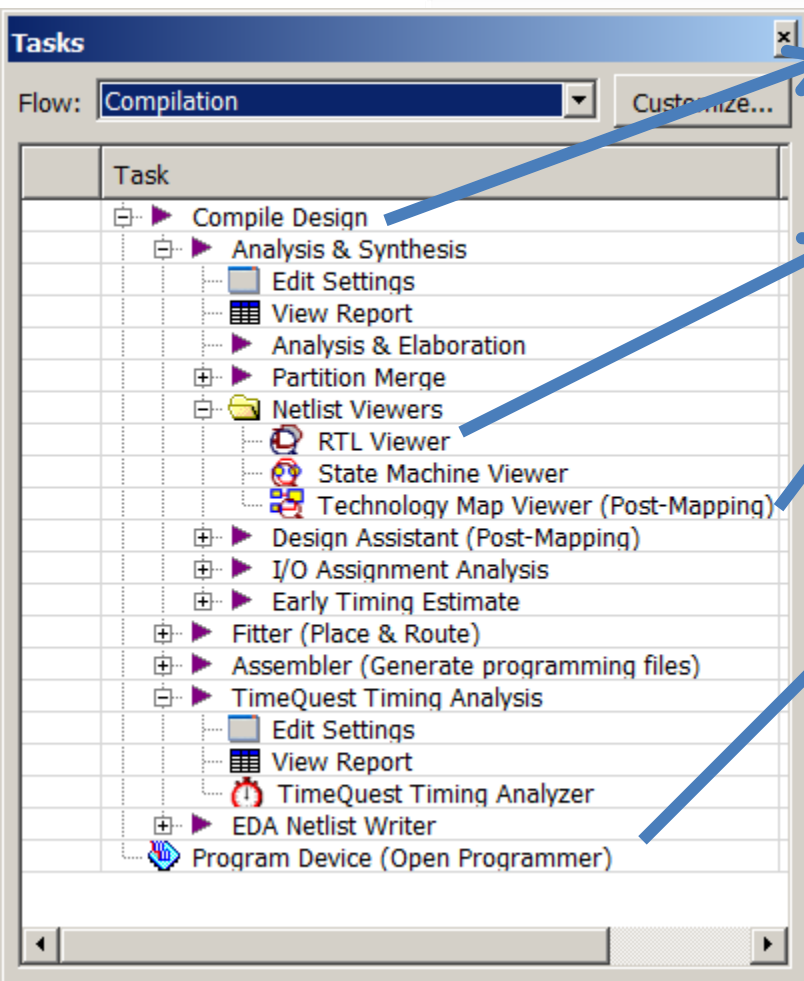
Quartus II – Getting started

- Ogni progetto DEVE contenere almeno una top-level entry (entità vhdl o schema a blocchi) che si chiama esattamente come il progetto.
- Le sue porte devono chiamarsi esattamente come i pin dell’FPGA che importate (vedi slide successive) oppure assegnato utilizzando il *pin planner*.



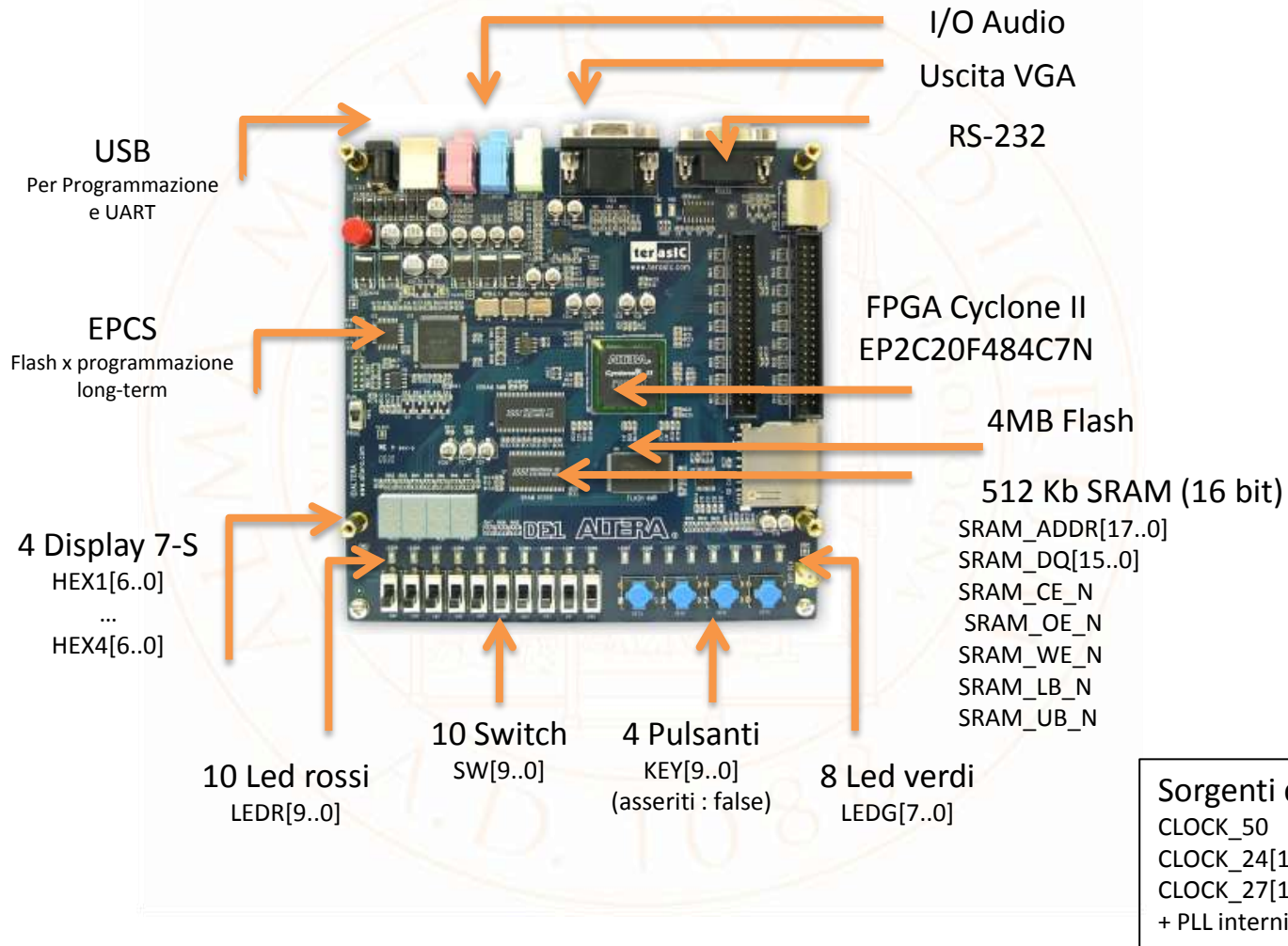
```
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4
5 entity nome_progetto is
6
7     port
8     (
9         a           : in  unsigned ((DATA_WIDTH-1) dc
10        b           : in  unsigned ((DATA_WIDTH-1) dc
11        clk          : in  std_logic;
12        sload        : in  std_logic;
13        accum_out    : out unsigned ((2*DATA_WIDTH-1)
14    );
15
16 end entity;
17
18 architecture RTL of nome_progetto is
19
20 ...
```


Flusso di sintesi



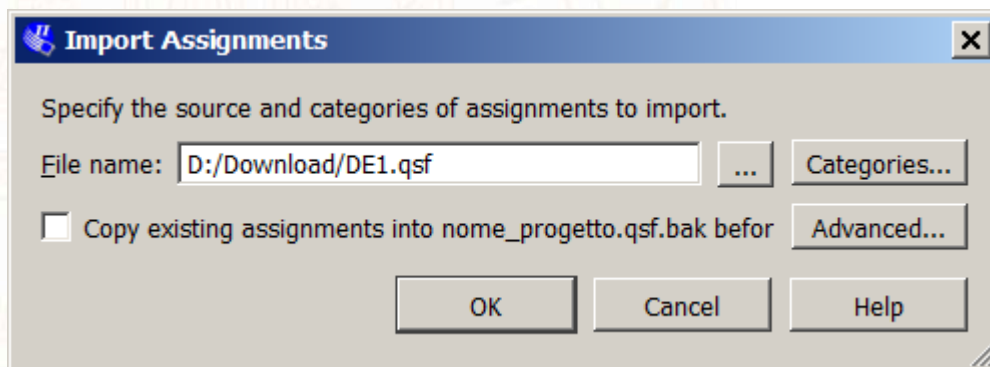
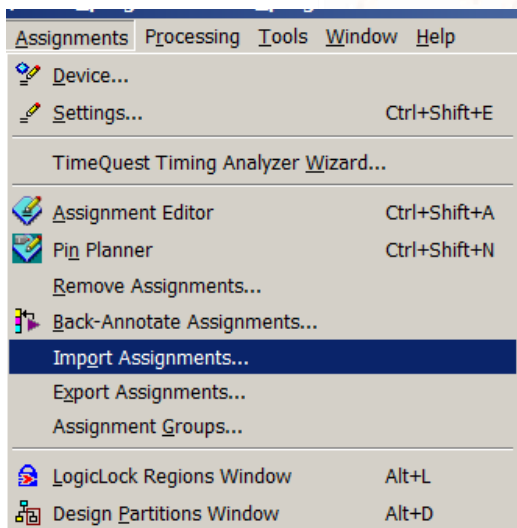
- **Compile Design**
Doppio click per sintetizzare e generare il file di programmazione
- **RTL Viewer**
Mostra la logica RTL inferita dal design (**UTILIZZATELO!**)
- **Technology Map Viewer**
Mostra il risultato del mapping sulle celle logiche dell'FPGA
- **Program Device**
Programma l'FPGA (in maniera volatile)

Schede dimostrative Terasic-Altera DE1



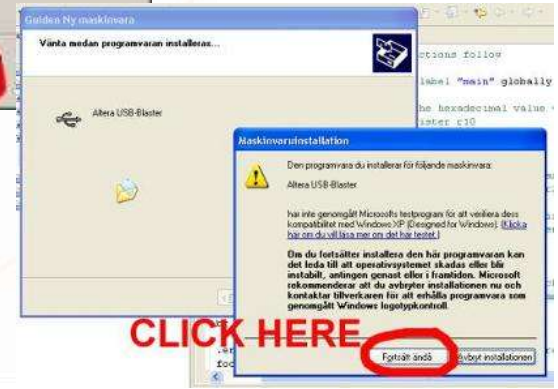
Mapping I/O FPGA su schede DE1

- Scaricare file con i mapping dei PIN I/O
ftp://ftp.altera.com/up/pub/Altera_Material/9.1/Boards/DE1/DE1.qsf
- Importare assignment nel progetto (menu Assignments → Import Assignments):
- Per i nomi dei PIN fate riferimento al file (DE1_Schematic.pdf) nello zip DE1 (o alla figura precedente)



Programmazione – Installazione driver

- Dopo aver collegato il cavo usb ed acceso la scheda, installate il driver della USB-blaster
- Percorso del driver: c:\Altera\10.1sp1\quartus\drivers\usb-blaster



Programmazione

- Task → Program Device (Open Programmer)

